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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,834	03/31/2004	Keiichiro Tounai	NEC A433	6044
27667 7590 07/17/2007 HAYES SOLOWAY P.C. 3450 E. SUNRISE DRIVE, SUITE 140 TUCSON, AZ 85718			EXAMINER PARK, EDWARD	
			ART UNIT 2624	PAPER NUMBER
			MAIL DATE 07/17/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/813,834

Applicant(s)

TOUNAI, KEIICHIRO

Examiner

Edward Park

Art Unit

2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 3/31/03
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____

DETAILED ACTION

Drawings

1. The drawings are objected to because of typographical errors in figure 2: “strat” appears to be “start”, “sanpling” appears to be “sampling”. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

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The following title is suggested: Method and Program for Correcting and Testing Mask Pattern for Optical Proximity Effect

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The USPTO "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" (Official Gazette notice of 22 November 2005), Annex IV, reads as follows:

Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.

When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) and *Warmerdam*, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory).

In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See *Lowry*, 32 F.3d at 1583-84, 32 USPQ2d at 1035.

4. **Claims 8-14** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter as follows. Claim 8 (and claims 9-14 by dependency) defines a program for causing a computer to carry out a method of testing a mask pattern embodying functional descriptive material. However, the claim does not define a computer-readable medium or memory and is thus non-statutory for that reason (i.e., "When functional descriptive

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material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized” – Guidelines Annex IV). That is, the scope of the presently claimed program for causing a computer to carry out a method of testing a mask pattern can range from paper on which the program is written, to a program simply contemplated and memorized by a person. The examiner suggests amending the claim to embody the program on “computer-readable medium” or equivalent in order to make the claim statutory. Any amendment to the claim should be commensurate with its corresponding disclosure.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 2, 3, 8, 9, 10, 15, 16, 17** are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al (US 6,907,596 B2).

Regarding **claim 1**, Kobayashi teaches a method of testing a mask pattern, comprising:

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applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (Kobayashi: figure 6c);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (Kobayashi: figure 6a-c);

determining sampling points on an edge of said first pattern (Kobayashi: figures 3b-d);

determining a test standard for each of said areas (Kobayashi: col. 6, lines 24-45);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (Kobayashi: col. 6, lines 24-45); and

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (Kobayashi: col. 6, lines 24-45), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (Kobayashi: col. 6, lines 46-67; col. 7, lines 1-30).

Regarding **claim 2**, Kobayashi teaches a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one ($N = 1, 2, 3, 4, \dots$), and first to N-th processes are different from one another (Kobayashi: col. 8, lines 20-34).

Regarding **claim 3**, Kobayashi teaches dividing an edge of said first pattern into a plurality of portions (Kobayashi: figures 6a-c), wherein said test standard is determined for each of said portions (Kobayashi: col. 6, lines 24-45).

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Regarding **claim 8**, Kobayashi teaches a program for causing a computer to carry out a method of testing a mask pattern, steps executed by said computer in accordance with said program (“central processing unit (CPU) 10 performs management of the entire mask data generating apparatus 100 and executes a control program stored in a main storage unit”;

Kobayashi: col. 6, line 4-7) including:

applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (Kobayashi: figure 6c);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (Kobayashi: figure 6a-c);

determining sampling points on an edge of said first pattern (Kobayashi: figures 3b-d);

determining a test standard for each of said areas (Kobayashi: col. 6, lines 24-45);

simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (Kobayashi: col. 6, lines 24-45); and

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (Kobayashi: col. 6, lines 24-45), wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (Kobayashi: col. 6, lines 46-67; col. 7, lines 1-30).

Regarding **claim 9**, Kobayashi teaches a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c).

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wherein N indicates an integer equal to or greater than one ($N = 1, 2, 3, 4, \dots$), and first to N-th processes are different from one another (Kobayashi: col. 8, lines 20-34).

Regarding **claim 10**, Kobayashi teaches dividing an edge of said first pattern into a plurality of portions (Kobayashi: figures 6a-c), wherein said test standard is determined for each of said portions (Kobayashi: col. 6, lines 24-45).

Regarding **claim 15**, Kobayashi teaches a method of testing a mask pattern, comprising:
applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer (Kobayashi: figure 6c);

dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer (Kobayashi: figure 6a-c);

determining sampling points on an edge of said first pattern (Kobayashi: figures 3b-d);
determining a test standard for each of said areas (Kobayashi: col. 6, lines 24-45);
simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern (Kobayashi: col. 6, lines 24-45); and

checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs (Kobayashi: col. 6, lines 24-45), and

transferring said mask pattern onto a mask (Kobayashi: col. 6, lines 24-45),
wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other (Kobayashi: col. 6, lines 46-67; col. 7, lines 1-30).

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Regarding **claim 16**, Kobayashi teaches a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one ($N = 1, 2, 3, 4, \dots$), and first to N-th processes are different from one another (Kobayashi: col. 8, lines 20-34).

Regarding **claim 17**, Kobayashi teaches dividing an edge of said first pattern into a plurality of portions (Kobayashi: figures 6a-c), wherein said test standard is determined for each of said portions (Kobayashi: col. 6, lines 24-45).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. **Claims 4, 5, 11, 12, 18, 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al (US 6,907,596 B2) in view of Tounai et al (US 2002/0043615 A1).

Regarding **claims 4 and 5**, Kobayashi discloses all elements as mentioned above in claim

1. Kobayashi does not teach a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer; and third area is comprised of said contact area and an ambient area surrounding said contact area.

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Tounai teaches a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (figure 13; Kobayashi: paragraphs [0093]-[0096]); and third area is comprised of said contact area and an ambient area surrounding said contact area (figure 13; Kobayashi: paragraphs [0093]-[0096]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Kobayashi reference to utilize a first pattern, second pattern, and a third area as suggested by Tounai, to fabricate/simulate a mask pattern and to increase reliability of correcting an optical proximity effect of the section around the contact area.

Regarding **claims 11 and 12**, Kobayashi discloses all elements as mentioned above in claim 8. Kobayashi does not teach a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer; and third area is comprised of said contact area and an ambient area surrounding said contact area.

Tounai teaches a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (figure 13; Kobayashi: paragraphs [0093]-[0096]); and third area is comprised of said contact area and an ambient area surrounding said contact area (figure 13; Kobayashi: paragraphs [0093]-[0096]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Kobayashi reference to utilize a first pattern, second pattern, and a third area as suggested by Tounai, to fabricate/simulate a mask pattern and to increase reliability of correcting an optical proximity effect of the section around the contact area.

Regarding **claims 18 and 19**, Kobayashi discloses all elements as mentioned above in claim 15. Kobayashi does not teach a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer; and third area is comprised of said contact area and an ambient area surrounding said contact area.

Tounai teaches a first pattern that is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer (figure 13; Kobayashi: paragraphs [0093]-[0096]); and third area is comprised of said contact area and an ambient area surrounding said contact area (figure 13; Kobayashi: paragraphs [0093]-[0096]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Kobayashi reference to utilize a first pattern, second pattern, and a third area as suggested by Tounai, to fabricate/simulate a mask pattern and to increase reliability of correcting an optical proximity effect of the section around the contact area.

9. **Claims 6, 7, 13, 14, 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al (US 6,907,596 B2) in view of Magoshi et al (US 6,316,163 B1).

Regarding **claims 6 and 7**, Kobayashi discloses all elements as mentioned above in claim

1. Kobayashi does not teach a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area.

Magoshi teaches a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area (figure 2; Magoshi: col. 5, lines 58-67; col. 6, lines 1-13).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Kobayashi reference to utilize a first pattern for forming a wiring layer, second pattern for forming an active area, and a fourth area comprised of a fifth area and an ambient area as suggested by Magoshi, to perform the steps of “forming patterns involving pattern transfer to the same photosensitive material” (Magoshi: col. 8, lines 32-45).

Regarding **claims 13 and 14**, Kobayashi discloses all elements as mentioned above in claim 8. Kobayashi does not teach a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained

by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area.

Magoshi teaches a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern, and a fourth area that is comprised of said fifth area and an ambient area surrounding said fifth area (figure 2; Magoshi: col. 5, lines 58-67; col. 6, lines 1-13).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Kobayashi reference to utilize a first pattern for forming a wiring layer, second pattern for forming an active area, and a fourth area comprised of a fifth area and an ambient area as suggested by Magoshi, to perform the steps of “forming patterns involving pattern transfer to the same photosensitive material” (Magoshi: col. 8, lines 32-45).

Regarding **claim 20**, Kobayashi discloses all elements as mentioned above in claim 8. Kobayashi does not teach a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Magoshi teaches a first pattern that is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern (figure 2; Magoshi: col. 5, lines 58-67; col. 6, lines 1-13).

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It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Kobayashi reference to utilize a first pattern for forming a wiring layer, and second pattern for forming an active area as suggested by Magoshi, to perform the steps of "forming patterns involving pattern transfer to the same photosensitive material" (Magoshi: col. 8, lines 32-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Park whose telephone number is (571) 270-1576. The examiner can normally be reached on M-F 10:30 - 20:00, (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner
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/Edward Park/

/Brian P. Werner/

Supervisory Patent Examiner (SPE), Art Unit 2624